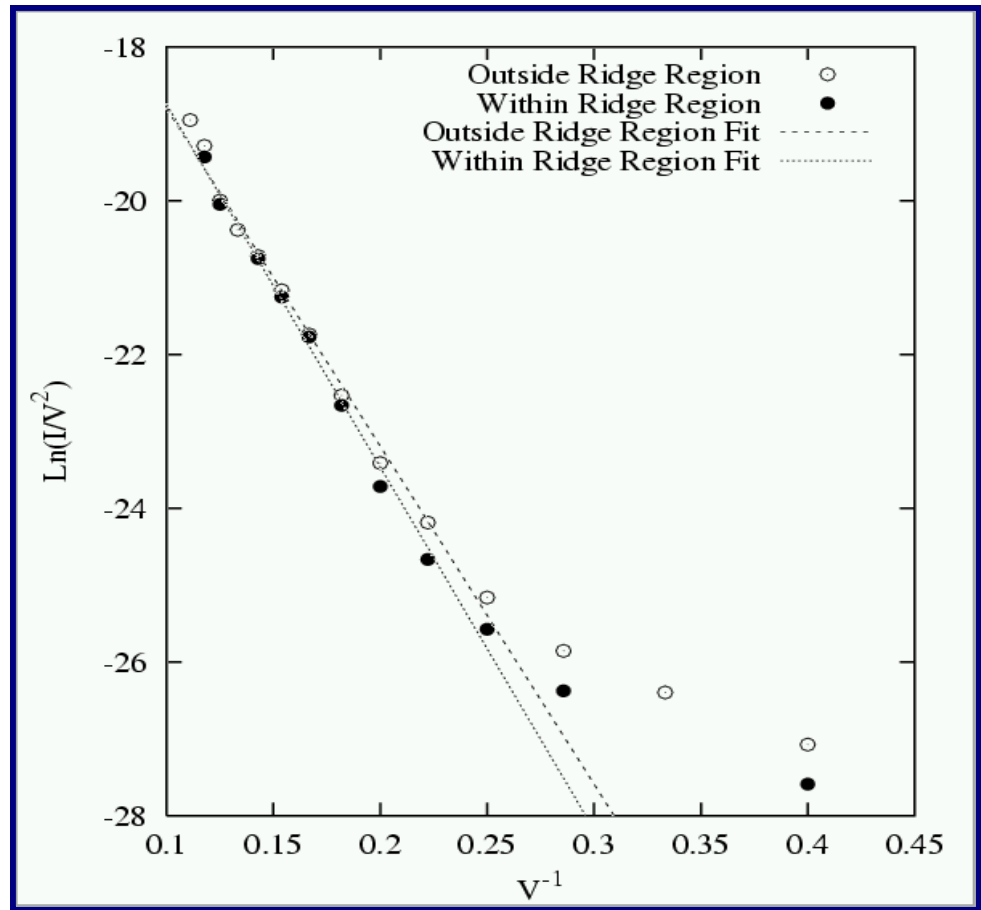
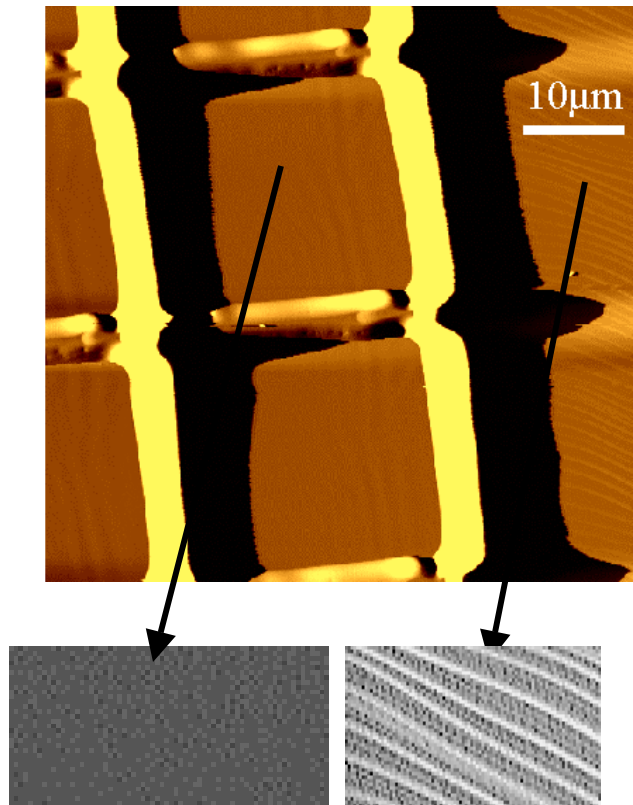


# Comparison of Device Structures on Atomically Flat Silicon and 'Normal' Silicon Wafer Surfaces



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Most electronic device structures are heterogeneous and consist of layers of different material in atomic contact. Many of these electronic device structures require high quality interfaces. Small, fast transistors use dielectric layers that are only a few atoms in thickness; the silicon surfaces on which those devices are built should ideally be atomically flat. We have developed a method for creating arrays of atomically flat silicon surfaces and have tested the performance of capacitor structures built on them in comparison with those on normal atomically rough surfaces. The slide shows AFM images (left) of areas (surrounded by ridges) of atomically flat (featureless) Si and normal atomically-stepped Si. The graph compares the leakage currents through capacitors built on the two types of surface. At an oxide thickness of a few nano-meters the leakage is by tunneling and is significantly less on the atomically flat surfaces. (Note the log scale). Future work will be aimed at scaling up the process to whole wafer dimensions and other device test structures.